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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,467	05/07/2004	Chc-Li Lin	12919-US-PA	3466

31561 7590 07/09/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
07/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/709,467	LIN, CHE-LI	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *6 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: *POL, CLK1, SHL, DIO2, DIO1, CLKN, CLKP, D22N, D22P, D01N, D01P, D00N, D00P, DATPOL* (see Figure 1). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not

accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "122" has been used to designate both source drivers and the data provided to the source drivers (e.g., see Figure 2); reference character "124" has been used to designate both gate drivers and the data provided to the gate drivers (e.g., see Figure 2); reference character "204" has been used to designate both source drivers and the data provided to the source drivers (e.g., see Figures 3 and 5); reference character "202" has been used to designate both gate drivers and the data provided to the gate drivers (e.g., see Figures 3 and 5).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 6 and 12 are objected to because of the following informalities: "driving" should be changed to "drive" (see line 3). Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Naito (US 6,462,735 B2)***.

Regarding claim 1, Naito discloses a color management structure for a panel display [Fig. 2; 400], comprising: a display array unit [Fig. 2; 410]; a plurality of gate drivers [Fig. 2; 420]; a plurality of source drivers [Fig. 2; 430], said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image; and a timing sequence control unit [Fig. 2; 200], said timing sequence control unit outputting a plurality of signals to said plurality of gate drivers and said plurality of source drivers to drive said display array unit (see Column 7, Line 30 - Column 8, Line 60), said timing sequence control unit outputting a clock signal [Fig. 9; 1008, CLK] and a color management data to said plurality of source drivers (see Column 15, Line 50 - Column 16, Line 31).

Regarding claim 2, Naito discloses said color management data is adjustable (see Column 12, Line 1-49).

Regarding claim 3, Naito discloses said panel display is a liquid crystal display (see Column 7, Line 10-15).

Regarding claim 4, this claim is rejected by the reasoning applied in rejecting claim 2; furthermore, Naito discloses said timing sequence control unit includes: a timing controller [Fig. 9; 1008] receiving a system input [Fig. 9; 1010] and providing said clock signal (see Column 15, Line 50 - Column 16, Line 31); and a color management control block [Fig. 2; 220], coupled to said timing controller, outputting said color management data and said clock signal to said plurality of source drivers, said color management data being adjustable (see Column 7, Line 30 - Column 8, Line 60).

Regarding claim 5, Naito discloses said color management control block includes: a storing unit [Fig. 1; 600] storing a color management basic data; and a processing unit [Fig. 1; 500] receiving said color management basic data and an output of said timing controller and outputting said color management data and said clock signal (see Column 7, Line 10 - Column 8, Line 60).

Regarding claim 6, Naito discloses each of said plurality of source drivers includes: a source drive circuit [Fig. 2; 430] to driving said display array unit; and a programmable data interface [Figs. 1 & 2; 200] receiving said color management data and said clock signal to parallel output a plurality of color voltage level signals to said source drive circuit (see Column 7, Line 30 - Column 8, Line 60).

Regarding claim 7, Naito discloses said plurality of color voltage level signals includes a plurality of color gamma voltage level data (see Column 8, Lines 42-60).

Regarding claim 8, Naito discloses said programmable data interface includes: an input interface [Fig. 1; input] receiving said color management data and said clock signal and translating [Fig. 1; 100] said color management data via a data format; a decoder [Fig. 1; 210] receiving said translated color management data and said clock signal and decoding said translated color management data, and outputting a decoded data [e.g., 10 bit data] and a control signal; and a digital-to-analog converting unit [Fig. 1; 260] receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals (see Column 8, Line 61 - Column 10, Line 15).

Regarding claim 9, Naito discloses said input interface [Fig. 2; 230] converts a serial input signal into a plurality of parallel output signals based on said clock signal (see Column 7, Line 10 - Column 8, Line 60).

Regarding claim 10, Naito discloses said digital-to-analog converting unit includes: a shift register receiving an output of said decoder; a latch receiving an output of said shift register and receiving said output of said decoder; and a plurality of digital-to-analog converters, coupled to said latch, corresponding to said plurality of color voltage level signals respectively (see Column 12, Line 60 - Column 13, Line 3).

Regarding claim 11, Naito discloses said timing sequence control unit is integrated into an application specified integrated circuit [Figs. 1 & 2; 210] (see Column 7, Line 30 - Column 8, Line 60).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claims 1 and 6; furthermore, Naito discloses a source driver [Fig. 2; 430] for driving a display array unit [Fig. 2; 410] of a panel display [Fig. 2; 400] (see Column 7, Line 30 - Column 8, Line 60), said source driver comprising: a source drive circuit to driving said display array unit; and a programmable data interface [Fig. 2; 200] receiving a color management data and a clock signal [Fig. 9; 1008, CLK] to parallel output a plurality of color voltage level signals to said source drive circuit (see Column 15, Line 50 - Column 16, Line 31).

Regarding claim 13, this claim is rejected by the reasoning applied in rejecting claim 7.

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claim 8.

Regarding claim 15, this claim is rejected by the reasoning applied in rejecting claim 9.

Regarding claim 16, this claim is rejected by the reasoning applied in rejecting claim 10.

Regarding claim 17, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Naito discloses a color management interface system [Fig. 2; 200], coupled to said timing sequence control unit and said plurality of source drivers, generating a color management data to said plurality of source drivers (see Column 7, Line 30 - Column 8, Line 60).

Regarding claim 18, this claim is rejected by the reasoning applied in rejecting claim 4; furthermore, Naito discloses said color management interface system includes a color management control block [Fig. 2; 220] in said timing sequence control unit and a color data converting unit [Fig. 2; 261] in each of said plurality of source drivers to obtain a plurality of color voltage level signals for said plurality of source drivers (see Column 7, Line 30 - Column 8, Line 60).

Regarding claim 19, this claim is rejected by the reasoning applied in rejecting claim 1.

Regarding claim 20, this claim is rejected by the reasoning applied in rejecting claim 9; furthermore, Naito discloses said color management data is a serial color management correction data (see Column 7, Line 10 - Column 8, Line 60).

Regarding claim 21, this claim is rejected by the reasoning applied in rejecting claims 1, 8, 9, and 20; furthermore, Naito discloses a color management method for a panel display [Fig. 2; 400], said panel display including a display array unit [Fig. 2; 410], a plurality of drivers [Fig. 2; 430], and a timing sequence control unit [Fig. 2; 200], said timing sequence control unit

outputting a plurality of signals to said plurality of drivers to drive said display array unit, said color management method comprising: generating a serial color management data via said timing sequence control unit (see Column 7, Line 10 - Column 8, Line 60), according to a clock signal (see Column 15, Line 50 - Column 16, Line 31); converting said serial color management data to a plurality of parallel analog color data signals (see Column 8, Line 61 - Column 10, Line 15); and inputting said plurality of parallel analog color data signals to said plurality of drivers to correct a color of a pixel (see Column 7, Line 30 - Column 8, Line 60).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Maeda et al (US 7,209,103 B2), Nishimura (US 7,173,599 B2), Chen et al (US 7,148,869 B2), Breier et al (US 7,144,335 B2), Yang (US 7,109,957 B2), Sakaguchi et al (US 7,088,324 B2), Matsuda et al (US 7,079,165 B2), Yoshida et al (US 7,002,594 B2), Maruoka et al (US 6,980,189 B2), Endo et al (US 6,961,035 B2), Yamazaki et al (US 6,909,411 B1), Dalal (US 6,801,179 B2), Endo et al (US 6,795,063 B2), Yamazaki et al (US 6,717,179 B1), Kobayashi et al (US 6,483,496 B2), Matsueda et al (US 6,384,806 B1), Yamazaki et al (US 6,335,716 B1), Chiang (US 6,271,822 B1), Van Mourik (US 6,215,468 B1), Kaburagi et al (US 6,160,532 A), and Yui et al (US 5,815,135 A) are cited to further evidence the state of the art pertaining to color management structures for panel displays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Piziali
25 June 2007